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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/625,010	07/22/2003	Kevin Weaver	100-22400 (PO5620)	8431	
33402	7590 09/29/2005		EXAMINER		
LAW OFFICES OF MARK C. PICKERING			HO, TU	HO, TU TU V	
P.O. BOX 300			ART UNIT	PAPER NUMBER	
PETALUMA,	CA 94933		2818	7.2 3.1 1.0 1.1 2.1	

DATE MAILED: 09/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

				<i>11'17</i>		
		Application No.	Applicant(s)			
Office Action Summary		10/625,010	. WEAVER ET AL.			
		Examiner	Art Unit			
		Tu-Tu Ho	2818			
Period f	The MAILING DATE of this communication app or Reply	pears on the cover sheet with the	correspondence address			
THE - External after - If the - If NO - Faile Any	MAILING DATE OF THIS COMMUNICATION. ensions of time may be available under the provisions of 37 CFR 1.13 r SIX (6) MONTHS from the mailing date of this communication. e period for reply specified above is less than thirty (30) days, a reply 0 period for reply is specified above, the maximum statutory period value to reply within the set or extended period for reply will, by statute 1 reply received by the Office later than three months after the mailing 1 red patent term adjustment. See 37 CFR 1.704(b).	36(a). In no event, however, may a reply be to y within the statutory minimum of thirty (30) dawill apply and will expire SIX (6) MONTHS from the application to become ABANDON	imely filed ys will be considered timely. In the mailing date of this communication ED (35 U.S.C. § 133).	n.		
Status						
1)⊠	Responsive to communication(s) filed on 12 So	eptember 2005.				
2a)⊠		action is non-final.				
3)[-					
	closed in accordance with the practice under E	Ex parte Quayle, 1935 C.D. 11, 4	53 O.G. 213.			
Disposit	ion of Claims		•			
5)⊠ 6)⊠ 7)□ 8)□	ion Papers	wn from consideration.				
·	The specification is objected to by the Examine		to buthe Evenines			
10)[The drawing(s) filed on <u>18 August 2003</u> is/are: Applicant may not request that any objection to the					
	Replacement drawing sheet(s) including the correct		• •	d).		
11)	The oath or declaration is objected to by the Ex	- · · · · · · · · · · · · · · · · · · ·		-,-		
Priority (under 35 U.S.C. § 119					
a)	Acknowledgment is made of a claim for foreign All b) Some * c) None of: 1. Certified copies of the priority documents 2. Certified copies of the priority documents 3. Copies of the certified copies of the prior application from the International Bureau See the attached detailed Office action for a list	s have been received. s have been received in Applica rity documents have been receiv u (PCT Rule 17.2(a)).	tion No red in this National Stage			
Attachmer	• •					
2) 🔲 Notio 3) 🔲 Infor	ce of References Cited (PTO-892) ce of Draftsperson's Patent Drawing Review (PTO-948) rmation Disclosure Statement(s) (PTO-1449 or PTO/SB/08) er No(s)/Mail Date	4) Interview Summar Paper No(s)/Mail [5] Notice of Informal 6) Other:				

Application/Control Number: 10/625,010 Page 2

Art Unit: 2818

DETAILED ACTION

1. Applicant's Amendment filed 09/12/2005 has been reviewed and placed of record in the

file.

2. Applicant's arguments with respect to amended claims 23 and 25, filed 09/12/2005, have

been considered but they are most in view of new ground(s) of rejection.

Claim Rejections § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 23 and 25 are rejected under 35 U.S.C. 103(a) as obvious over Akram et al. U.S.

Patent 6,022,750 (the '750 reference, cited in a previous office action) in view of KISHIMOTO

et al. U.S. Patent Application Publication 20010048980 (the '980 reference, cited in a previous

office action).

The '750 reference discloses in Figs. 2-14 and respective portions of the specification a

semiconductor device substantially as claimed.

Referring to claim 23, the reference discloses a semiconductor device comprising:

a die (12, column 4, first paragraph); and

a test structure (16, Figs. 2-4 and 12) including capacitive test element 118 (Fig. 12,

columns 4 through column 7, particularly paragraph bridging columns 4 and 5 and column 7,

lines 53-60) that contacts a top surface of the die.

However, the '750 reference does not disclose structural details of the die 12. The reference further fails to disclose that the die comprises a multilevel interconnect structure as claimed.

Nevertheless, KISHIMOTO, in disclosing also a semiconductor die, as noted in section A-b of the office action mailed 06/08/2005, teaches that a semiconductor die should comprise multilevel interconnections and inter-layer insulators to increase density.

Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the reference's die with a multilevel interconnections. One would have been motivated to make such a change because a die including a multilevel interconnection structure has increased density.

The capacitive test element 118 of the semiconductor device of the '750 reference including a die such modified would comprise said interconnect structure and further comprise:

a first conductive region (118 or 120, column 7, lines 53-60, of the capacitive test element 118 as applied to the semiconductor device of Fig. 4) having a first surface adhered to an exterior surface of the interconnect structure (including test pad 62 as depicted in Fig. 4) and an opposing second surface;

an insulation region (122) having a first surface and an opposing second surface, the first surface of the insulation region contacting the second surface of the first conductive region; and a second conductive region (120 or 118) having a first surface and an opposing second surface, the first surface of the second conductive region contacting the second surface of the insulation region, the second conductive region being electrically isolated from the first conductive region.

Art Unit: 2818

Referring to **claim 25**, the semiconductor device such modified including such modified die would further comprise all limitations as detailed in the office action mailed 06/08/2005 in section A-c. Specifically, the semiconductor device including the die would comprise:

a first opening formed in the dielectric structure (such as 20, the Downey reference) of the die, the first opening extending from the top surface down to a first region on a metal interconnect (such as 21,22,23); and

a first conductive structure formed in the first opening to make an electrical contact with the first region, and on the top surface to make an electrical contact with the test structure (more specifically to the capacitive test element 118 of the test structure of the '750 reference to make an electrical contact with the first region so that the capacitive test element 118 functions as a capacitive test element);

In order for the capacitor test structure, which comprises two terminals, to function, a second opening should be formed in the dielectric structure to reach a second region of the metal interconnect, and a second conductive structure formed in the second opening to make an electrical contact with the second region, and on the top surface to make an electrical contact with the test structure. Alternatively, the semiconductor device including the die and the test structure (16, Figs. 3 and 5-14) including other test elements such as 80, 82, 74, 78, ...should comprise at least a second opening formed in the dielectric structure to reach a second region of the metal interconnect, and a second conductive structure formed in the second opening to make an electrical contact with the second region, and on the top surface to make an electrical contact with the test structure including the various test elements so that the various test elements function as test elements.

Application/Control Number: 10/625,010 Page 5

Art Unit: 2818

Allowable Subject Matter

4. Claims 2, 4-10, and 28-37 are allowable over the prior art of record. The allowable subject matter including that which was indicated in the previous office action and/or as amended in claims 2 and 29.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office Action. See MPEP § 706.07(a).

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Application/Control Number: 10/625,010 Page 6

Art Unit: 2818

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The

examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho

September 24, 2005